A High Speed ATM Switch with Random Access Input Buffers

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1. Introduction

There have been proposed some ATM switches which are willing to be applied to high-speed BISDN network[1]. In this paper, we propose a new high-speed ATM switch which uses a common buffer for each input buffer. The proposed switch, named RAIB (Random Access Input Buffer) switch, also uses several ABs (Address Buffers) in every input module to manage common buffer in the same module. An arbiter for a given output controls ABs for the same output. Through computer simulation, we found out that our proposed ATM switch was significantly improved in the view point of cell loss probability characteristics, comparing with a conventional input switch.

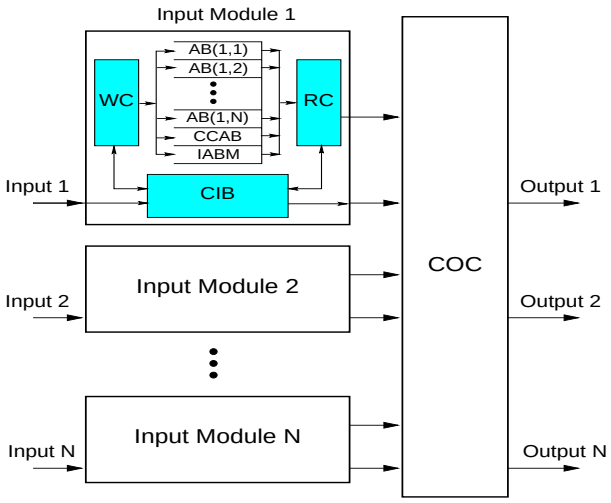

Figure 1: Schematic diagram of RAIB switch.

2. Switch Architecture

Figure 1 shows the schematic diagram of RAIB switch[2]. It consists of a bank of input modules and a common output controller (COC). When a cell arrives at an input module, the write controller (WC) checks the header of the arriving cell and saves it at a common input buffer (CIB) which is a fully-shared common buffer. An address buffer (AB) stores the addresses of CIB where arriving cells are saved. If arriving cell is a multicasting cell, the address of CIB is stored at the cell copy address buffer (CCAB). An idle address bit map (IABM) is used for designating the unused buffer space. A read controller retrieves a cell from one of AB or CCAB depending on the result of arbitration which is executed in COC. COC consists of a space switch such as a crossbar switch and an arbitration logic. The arbitration is performed for each output by similar round-robin.

3. Simulation

We assume that cell arrivals on the N input ports are governed by independent and identical Bernoulli process. Each cell has equal probability $1/N$ of being switched to any given output. Figure 2 shows the cell loss probability of the RAIB switch for different switch size. The buffer space is assumed as three times the switch size. For example, for the 8×8 switch, 24 cell-size buffer is usde for each input.

4. Conclusions

In this paper, we proposed a new high-speed ATM switch named RAIB. We use a common buffer and multiple address buffers in each input. Computer simulation shows that the proposed ATM switch significantly improved performance characteristics comparing with conventional input switch.

References

[1] Sang H. Kang, Changhwan Oh, and Dan K. Sung, "A High Speed ATM Switch with Common Parallel Buffers," Proc. of Globecom '95, pp. 2087-2091, 1995.

[2] Hakyong Kim, Changhwan Oh, and Kiseon Kim, "A High Speed ATM Switch Architecture with Random Access Input Buffers," Proc. of JCCI'96, pp. 240-244, 1996. (in Korean)

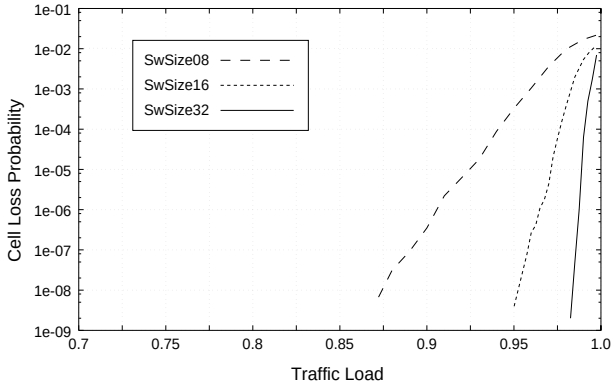

Figure 2: Schematic diagram of RAIB switch.