Throughput Analysis of MIQ Switches

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Abstract— **The multiple input-queued (MIQ) switch is the switch which manages multiple (m) queues in each input port, each of which is dedicated to a group of output ports. Since each input port can attend m arbitration rounds, the switch suffers from a reduced HOL blocking which is known as the decisive factor limiting the throughput of the pure single input-queued (SIQ) packet switch. As the result, the MIQ switch guarantees satisfying performance characteristics as the number of queues m increases. However, the service of multiple cells from an input could cause the internal speedup or expansion of the switch fabric, diluting the merit of high-speed operation in the conventional SIQ scheme. The restricted rule is contrived to circumvent this side effect by regulating the number of cells switched from an input port to just one cell. In this paper we analyze the performance of MIQ ATM switch employing the restricted rule. For the switch using the restricted rule, the closed formulae for the throughput bound of the switch are derived as the function of m, by generalizing the analysis for the SIQ switch by Hui *et al.* [1].**

Keywords— **Multiple input-queueing, MIQ, ATM switch.**

I. Introduction

IT is the well-known fact that the throughput of the single input-queued (SIQ) packet switch is limited to 0.586 for an independently and identically distributed Bernoulli arrival traffic with the cell destinations uniformly distributed over all output ports, namely the homogeneous Bernoulli arrival traffic, when the switch size is infinite [1], [2]. In order to overcome the throughput limit of the SIQ switch, many alternative queueing methods and/or scheduling schemes have been engineered such as window policy, input smoothing, and the multiple input-queueing schemes [2]-[6]. The essence of these schemes is to allow one of cells behind the HOL cell to be switched to an idle output when the HOL cell is blocked, or to allow multiple cells to be the HOL cell and thereby increases the opportunity for an input to serve a cell or cells. Among those schemes, the multiple input-queueing scheme is drawing much attention recently in that it can provide both high-speed operation and high switching performance.

The multiple input-queued (MIQ) switch is the switch equipped with multiple queues in every input. Since the queues are independent logically or physically of other queues in the same input, an input can switch plural cells in a time slot, which leads to the internal speedup or to the switch fabric expansion though. The *restricted rule* is come up with to resolve such problems in the MIQ switch. The rule regulates an input to switch at most one cell in a time slot. Restricting the number of cells to be switched, in a sense, implies that the maximum achievable performance may be degraded a little bit but makes it feasible to develop the high-speed and high-performance ATM switch.

In connection with the restricted rule, many scheduling algorithms have been suggested [7]-[11], and some of them compensate the performance degradation caused by the restricted rule by finding maximum matching between input and output ports. Another cardinal issue related to the restricted rule is the implementation and time complexity of the scheduling algorithm.

In this paper, we will focus on the performance side of the MIQ switch rather than other issues, since there is a limited number of studies on the performance analysis for the MIQ switch [12]-[17] and, if any, most of the studies apply only to a particular MIQ switch called the virtual output-queued switch. We first develop the queueing model for the multiple input-queued switch employing the restricted rule and then analyze the performance measures of the switch by generalizing the analysis results for the SIQ packet switch [1].

This paper is organized as follows: In Section II, we investigate the concept of multiple input-queueing and two types of cell selection rules: the restricted rule and the free rule. In Sections III, throughput of the MIQ switch is analyzed in terms of the number of queues in an input port and the offered load. Finally, we conclude this paper in Section IV with the discussion on the application of the switch in the future broadband communications systems.

II. Multiple Input-Queued ATM Switch

Comparing with the output-queued switch, the single input-queued (SIQ) switch has an inherent merit that it operates at the same speed as the external link speed, making the input-queued switch more suitable for the high-speed switching system. Moreover, the input queueing is considered easier to implement in hardware than its output-queued-counterpart. On the other hand, the input-queued switch suffers from the HOL blocking so that its maximum attainable throughput is limited to 0.586 for the homogeneous traffic [1], [2]. Therefore, many buffering and scheduling schemes have been conceived to overcome the throughput limit of the SIQ switch. They fall into five large categories: (i) examining the first k packets in a FIFO queue instead of the HOL packet only. This scheme is called *window policy*, or sometimes called as look-ahead scheme or bypass scheme; (ii) expanding the internal switch bandwidth either by enlarging the switch dimension or by replicating the switch fabric. This scheme is called *input smoothing* or *input expanding*; (iii) employ-

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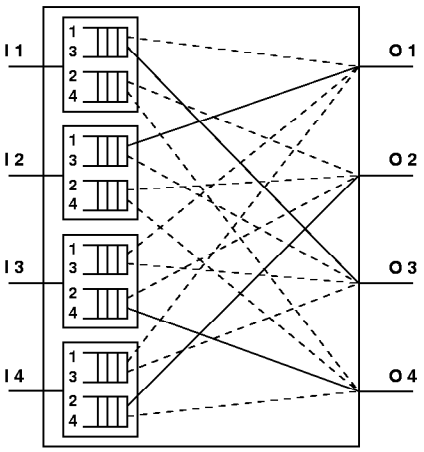

Fig. 1. The multiple input-queued ATM switch.

ing multiple FIFO queues instead of a single FIFO in every input port. This scheme is referred to as the *multiple input-queued (MIQ) scheme* or *bifurcated input-queued scheme*; (iv) dropping or discarding the blocked HOL cells in the FIFO queue; (v) input grouping or trunking. Among them, it is reported that the MIQ scheme can dramatically improve the switching performance, and thus, lift the throughput bound of the SIQ switch up to 1.0 when the number of queues in an input is equal to the switch size [9], [19].

Among them, the multiple input-queueing scheme, as shown in Fig.1, is the idea of deploying multiple (m) FIFO queues in each input port, each of which is dedicated to a group of output ports. When m is equal to one, that is, the single queue is dedicated to all output ports, the MIQ switch corresponds to the conventional SIQ switch. When m is equal to the switch size N, that is, each queue is dedicated to a specific output port, the MIQ switch is referred to as the virtual output-queued (VOQ) switch. It is reported that the performance characteristics of the MIQ switch is improved with m [12], [14], [19].

The value of m is usually taken to be one of 2's powers (1, 2, 4, 8, $\cdots$) in the range from 1 to N and N is assumed to be the multiple of m. Therefore, each queue stores cells for N/m output ports exclusively and exhaustively. That is, output groups do not overlap with others in terms of output ports. Then, we can here make an important observation that the switch can be split into m identical subswitches whose size is $N \times N/m$ and each subswitch corresponds to an output group [1]. Then, the MIQ switch can switch up to m cells from an input port in a time slot since an input port manages m physically or logically distinct queues. However, the total number of cells switched from all inputs must not exceed N and each output can receive at most one cell in every time slot since there is no queue at output port. Even though the service of multiple cells from an input port is an essential reason of the performance enhancement in the MIQ switch, it gives rise to the internal speedup (or the expansion in the switch fabric) at the same time, diluting the salient merit of the input-queued switch. The internal speedup makes the switch not to be suitable for the high-speed and high-performance switch and, for the reason, it is one of the important issues to be resolved for future switching systems.

Therefore, most scheduling schemes developed for the MIQ switch assume that each input can switch at most one cell in a time slot. The rule governing this assumption is referred to as *the restricted rule* [2] [18], [19]. Under the restricted rule, the switch thus operates at the same speed as the external link speed. On the other hand, *the free rule* allows an input port to switch up to m cells in a time slot with the potential internal speedup provided that the total number of switched cells is no more than N. In [19], the authors showed that (1) the saturation throughput of the MIQ switch converges to 1.0 as m increases irrespective of the rules employed and that (2) the free rule yield slightly higher saturation throughput for moderate values of m.

The performance for the free rule has been evaluated through different analytical ways in [12]-[16]. In Reference [13], the authors derived the closed expression for the saturation throughput of the MIQ switch using the free rule in terms of the number of queues in an input by simply extending Hui's result in [1]. In Reference [14], the author did the same work by generalizing Karol's result in [2]. However, performance of the restricted rule has been usually evaluated through computer simulation since input ports and their queues are mutually dependent on one another in regulating the number of cells switched from each input. In [17], the authors just provided an anlysis result for the restricted rule by extending the results in [1] and, in [20], the author reused the same analysis procedure and result found in [17]. In the following section, we analyze the performance of the MIQ switch employing the restricted rule in a heuristic manner after developing a queueing model for a queue.

III. Saturation Throughput

In this section, we first develop a queueing model for an MIQ switch using the restricted rule as the contention resolution scheme and then analyze it analytically in terms of the saturation throughput.

A. Queueing model for the throughput

For the MIQ switch which we analyze in the following subsection, we assume that the switch size is $N \times N$ and the number of FIFO queues in an input port is m ($1 \leq m \leq N$). That is, each queue stores the packets for N/m output ports, where N/m should be an integer number. The interconnection network of the switch is internally nonblocking as the crossbar switch. For the switch, we assume further that time is slotted and the slots carry fixed-length packets like ATM cells. In this paper, we will use *cell* for the fixed-length packet. Cells arrive at input

[1] The words of subswitch and output group will be used interchangeably in this paper.

[2] A similar rule to the restricted rule is found in [20] where the author referred it to as 'single write'.

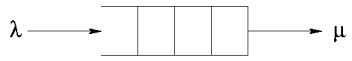

Fig. 2. Queueing model for an input of the MIQ switch.

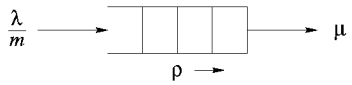

Fig. 3. Queueing model for a queue.

ports or queues just after the time boundaries, and depart from the input ports or queues just before the time boundaries. Namely, the early-arrival model [21]. Traffics arriving at each input are assumed to be independent and identical to one another. The arrived traffics are assumed to be uniformly distributed for N outputs. In other words, uniformly distributed for m queues in an input port. We refer this kind of traffics to *the homogeneous Bernoulli arrival traffic*. During a time slot, each input can switch no more than one cell and each output can receive at most one cell.

For the MIQ switch of interest, let the mean arrival rate and the mean service rate for an input port be λ and μ, respectively, as shown in Fig. 2. In an input port, then, the mean arrival rate for a queue becomes λ/m since the arrived traffic is distributed uniformly between m queues. On the other hand, the mean service rate for a queue is still μ. Therefore, the resulting queueing model for a queue can be represented as shown in Fig. 3. In the figure, let ρ be the steady-state probability that a queue has a fresh HOL cell which is just moved to the HOL position, given that the queue is not blocked during the previous slot. The fresh HOL cell means the cells that move up to the HOL position [1]. They were either queued or, if the queue was empty, they are new.

B. Saturation throughput for the restricted rule

As mentioned before, arbitrations are assumed to be performed sequentially for each output group or subswitch and input ports selected in earlier arbitrations should be excluded in later arbitrations for remaining output groups or subswitches in some ways. Differently from the MIQ switch using the free rule, the throughput for subswitches or output groups is different from one another in the MIQ switch using the restricted rule since later arbitrations are dependent on the result of previous arbitrations [18]. Therefore, the throughput for the entire switch can be obtained by taking expectation on the sum of the throughputs for m output groups or subswitches.

We number output groups from 1 to m where the output group including the first N/m output ports is referred to as output group 1. For convenience, let us assume that the arbitration starts from output group 1. Letting T_1 designate the throughput for the first $N \times N/m$ subswitch corresponding to output group 1, then T_1 becomes

$$T_1 = \frac{m}{N} \sum_{j=1}^{\frac{N}{m}} E[\epsilon(N_j)] = E[\epsilon(N_j)] \tag{1}$$

where the indication function $\epsilon(x)$ is

$$\epsilon(x) = \begin{cases} 1, & x \geq 1 \\ 0, & x = 0 \end{cases}$$

and N_j is the number of HOL request for the same output port j. As long as m is not equal to N, the MIQ switch suffers from the HOL blocking as mentioned in Section II, the state of HOL blocking is characterized by N_j. Note here that the index j for output ports in Eq. (1) takes its value between 1 and N/m since the arbitration for output group 1 concerns the first N/m output ports in output group 1. The number of all HOL cells that became blocked at the end of a slot, $N^{(b)}$, is

$$N^{(b)} = \sum_{j=1}^{\frac{N}{m}} N_j - \sum_{j=1}^{\frac{N}{m}} \epsilon(N_j) \,. \tag{2}$$

Taking expectation on both sides of Eq. (2) and combining it with Eq. (1), then we get

$$T_1 = E[N_j] - \frac{m}{N} E\left[N^{(b)}\right] \,. \tag{3}$$

We can get T_1 by computing the last two terms in Eq. (3) in terms of λ_1, respectively, since we have $T_1 = \lambda_1$ in steady state. Note that λ_1 is the mean or effective arrival rate for output group 1.

Two terms in the righthand side of Eq. (3) can be obtained directly from the analysis of the SIQ switch in [1]:

$$E[N_j] = \lambda_1 + \frac{\lambda_1^2}{2(1-\lambda_1)} \tag{4}$$

and

$$E\left[N^{(b)}\right] = \frac{N}{m}\left(m - \frac{\lambda_1}{\rho}\right) \,. \tag{5}$$

Substituting Eqs. (4) and (5) into Eq. (3), we have the throughput for the first N/m output ports (or for output group 1):

$$T_1 = \lambda_1 + \frac{\lambda_1^2}{2(1-\lambda_1)} - \frac{m}{N}\left(N - \frac{N}{m}\frac{\lambda_1}{\rho}\right)\Big|_{\lambda_1 = T_1} \tag{6}$$

from which we obtain the equation

$$(2-\rho)T_1^2 - 2(m\rho+1)T_1 + 2m\rho = 0 \tag{7}$$

or

$$T_1 = \frac{m\rho + 1 - \sqrt{(m\rho+1)^2 - 2m\rho(2-\rho)}}{(2-\rho)} \,. \tag{8}$$

The saturation throughput for output group 1 is obtained by setting $\rho = 1$ in Eq. (7), and

$$T_{1,sat} = m + 1 - \sqrt{m^2+1} \,.$$

Letting S_1 designate the number of input ports selected in the arbitration for output group 1, it becomes

$$S_1 = \frac{N}{m} T_1 \,.$$

Now, let us turn our attention to output group 2. The number of output ports in output group 2 is still N/m, and hence, Eqs. (1) through (3) can be used without any modifications for output group 2 except for the suffix. In the arbitration for output group 2, however, the number of unblocked queues, R_2, changes into

$$R_2 = (N - S_1) - N^{(b)} \tag{9}$$

since we prevent S_1 input ports, selected in the arbitration for output group 1, from attending the arbitration for output group 2. That is, the term $(N - S_1)$ of Eq. (9) designates the number of input ports (or queues) which is eligible for attending the arbitration for output group 2. Taking expectation on both sides of Eq. (9) and using the flow conservation rule of $E[R_2]\rho = (N/m)\lambda$, we have

$$\begin{aligned} E[N^{(b)}] &= N - E[S_1] - \frac{N}{m}\frac{\lambda_2}{\rho} \\ &= N - \frac{N}{m}\delta_1 - \frac{N}{m}\frac{\lambda_2}{\rho}\,, \end{aligned} \tag{10}$$

where $\delta_1 = \lambda_1$. Substituting Eqs. (4) and (10) into Eq. (3), we get

$$(2-\rho)T_2^2 - 2((m-\delta_1)\rho + 1)T_2 + 2(m-\delta_1)\rho = 0\,. \tag{11}$$

Throughput for output group 2 T_2 is obtained by solving Eq. (11). Setting $\rho = 1$ in Eq. (11), we immediately have the saturation throughput for output group 2:

$$T_{2,sat} = m - \delta_1 + 1 - \sqrt{(m-\delta_1)^2 + 1}\,.$$

The same reasoning can be used for output group 3 and later uptil output group m when m is greater than or equal to 3. Then, the number of unblocked queues becomes

$$R_i = \left(N - \sum_{j=1}^{i-1} S_j\right) - N^{(b)}$$

where

$$S_j = \frac{N}{m}T_j\,.$$

When the offered load to an input port is ρ, the throughput for output group i is

$$(2-\rho)T_i^2 - 2((m-\delta_{i-1})\rho + 1)T_i + 2(m-\delta_{i-1})\rho = 0 \tag{12}$$

or

$$T_i = \frac{(m-\delta_{i-1})\rho + 1 - SQRT_i}{2-\rho}\,, \tag{13}$$

where

$$SQRT_i = \sqrt{((m-\delta_{i-1})\rho + 1)^2 - 2\rho(2-\rho)(m-\delta_{i-1})}$$

and

$$\delta_i = \begin{cases} 0, & i = 0 \\ \sum_{j=1}^{i} T_j\,, & i \geq 1. \end{cases}$$

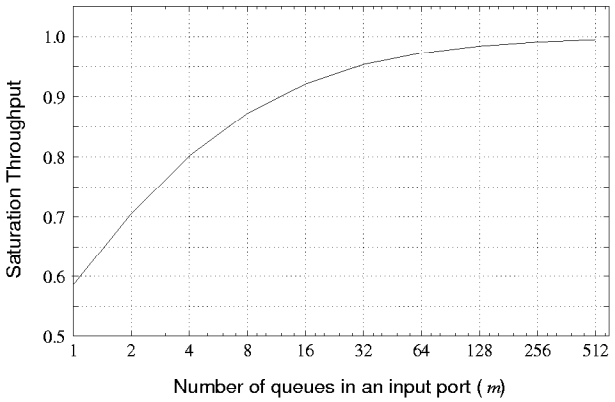

Fig. 4. The saturation throughput of the MIQ switch employing the restricted rule.

The saturation throughput for output group i is expressed by setting $\rho = 1$ as

$$T_{i,sat} = m - \delta_{i-1} + 1 - \sqrt{(m-\delta_{i-1})^2 + 1}\,. \tag{14}$$

Consequently, the average throughput of the MIQ switch using the restricted rule is given by

$$T_{sat} = \frac{1}{m}\sum_{i=1}^{m} T_{i,sat} = \frac{1}{m}\delta_m\,. \tag{15}$$

Note that the resulting equstions Eq. (14) and Eq. (15) take the similar form to those in [17]. The total saturation throughput is also given by Eq. (15) with setting $\rho = 1$.

Figure 4 plots the saturation throughput of the MIQ ATM switch employing the restricted rule for different values of m. The figure shows that the saturation throughput converges to 1.0 as the number of queues m increases. Note that the saturation throughput for the restricted rule is slightly lower than that for the free rule since each input is regulated to serve at most one cell under the restricted rule in [13] and [19]. Table I shows the saturation throughput for different values of m, as well as δ_m.

Considering the MIQ switch under the free rule, all inputs can attend all arbitration rounds in the same time slot even though they are selected once or more in previous arbitrations. It implies that the throughput for every arbitration is equal to that for the first arbitration of the restricted rule. Then, the throughput of the MIQ switch using the free rule is equal to Eq. (8) except the suffix:

$$T_{free} = \frac{m\rho + 1 - \sqrt{(m\rho+1)^2 - 2m\rho(2-\rho)}}{2-\rho}\,. \tag{16}$$

The saturation throughput is obtained by setting $\rho = 1$ in Eq. (16):

$$T_{free,sat} = m + 1 - \sqrt{m^2 + 1}\,, \tag{17}$$

and tabulated in Table I together with the saturation throughput for the restricted rule. Eq.(17) agrees with the result in [14].

TABLE I

SATURATION THROUGHPUTS T_{sat} AND δ_m FOR DIFFERENT VALUES OF m. λ IS OBTAINED BY DIVIDING δ_m WITH m. $T_{free,sat}$ IS THE SATURATION THROUGHPUT FOR THE FREE RULE.

m	T_{sat}	δ_m	$T_{free,sat}$
1	0.586	0.586	0.586
2	0.705	1.410	0.764
4	0.802	3.206	0.877
8	0.873	6.981	0.938
16	0.921	14.738	0.969
32	0.953	30.482	0.984
64	0.972	62.215	0.992
128	0.984	125.939	0.996
256	0.991	253.656	0.998
512	0.995	509.367	0.999

IV. CONCLUSIONS

In this paper, we investigated the multiple input-queued (MIQ) ATM switch. Differently from that the conventional single input-queued (SIQ) switch having a single queue in each input, the MIQ switch has m ($1 \leq m \leq N$) queues in each input. Each of the queues is dedicated to a group of output ports. Since the MIQ switch equips m logically or physically distinct queues in each input, it could serve up to m cells from an input in a time slot. The rule governing this multiple-cell service is referred to as the free rule. However, the multiple-cell service requires the internal speedup in the switch fabric or in the interfaces between input modules and the switch fabric, or more sophisticated hardware additionally. Therefore, most studies on the MIQ switch assumes that at most one cell can be served from an input port. This assumptions is referred to as the restricted rule.

Under the free rule, the cell selection for outputs is independent of input ports since multiple cells can be served from an input irrespective of other inputs. Under the restricted rule, however, the cell selection is dependent on other inputs' decision when we assume that the cell selections for all outputs occur sequentially. Therefore, we can evaluate the performance measures in the average form or by using average parameters. In this paper, we derived the throughput of MIQ switches in terms of the number of queues m and the offered load λ. The analysis results show that the saturation throughput of the restricted rule approaches 1.0 as m goes to infinite even though it is slightly less than that of the free rule.

In addition to the enhanced switching performance, the MIQ switch employing the restricted rule operates at the same speed as the external link speed. It implies that the switch is appropriate for the high-speed switching systems or gigabit routers requiring high performance as well as broder switching bandwidth.

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