LETTER

Throughput Analysis of the Bifurcated Input-Queued ATM Switch

Hakyong KIM[†], *Nonmember*, **Changhwan OH**[†], *Member*, **Yongtak LEE**[†], *and* **Kiseon KIM**[†], *Nonmembers*

SUMMARY In this paper there suggested is a bifurcated (or multiple) input-queued ATM switch in which a buffer for each input port is divided into multiple (m) buffer blocks, i.e., bifurcated buffers, for enhancement of the limited throughput of the ordinary input-queued switch using a single FIFO. As the contention/arbitration rule for the bifurcated input-queued switching scheme, free and restricted contention rules are come up with and discussed. The free rule allows an input port to switch up to m cells at the cost of internal speedup. With the restricted rule, on the other hand, an input port can switch no more than one cell in a time slot so that the switch operates at the same speed as the external link speed. The throughput bound for the bifurcated input-queued switch is analyzed for both rules through the generalization of the analysis by Karol *et al* [1]. The throughput bound approaches to 1.0 as m becomes large enough, irrespective of the contention/arbitration rule.

key words: bifurcated input-queued ATM switch

1. Introduction

For the independent and uniform arrival traffic, the saturation throughput of an input-queued non-blocking packet switch is asymptotically upper bounded by 0.586 as the switch size (N) becomes infinite [1], [2], while the output-queued switch attains 100% throughput irrespective of the switch size. Therefore, many approaches have been proposed to improved the limited throughput of the traditional input-queued switch with a single FIFO. Those approaches could achieve sizeable enhancement in the maximum achievable throughput by mitigating the HOL blocking effect through peculiar buffer management schemes and/or arbitration methods. However, they also resulted in such internal speedup as in the output-queued switch [3].

One successful idea for the throughput enhancement of the input-queued packet switches with a single FIFO is a *bifurcated input-queueing* or *multiple input-queueing* approach. In the input-queueing approach which is a kind of input smoothing, each input port equips and manages m FIFOs called the *bifurcated buffer* ($1 \leqq m \leqq N$). The bifurcated buffer originally means, as the name implies, the buffers divided into two. The term, however, can be used as the extension of the bifurcation concept even when the number of buffers is larger than two [3]-[5]. The bifurcation approach, in general, pulls the throughput bound up to 1.0 as the number of bifurcated buffers in an input port (m) gets close to the switch size (N).

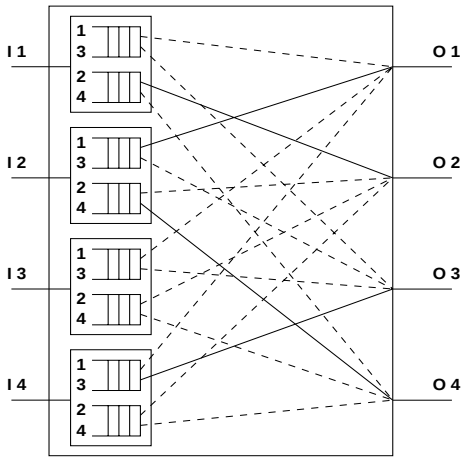

Fig. 1 A 4×4 bifurcated input-queued switch with free contention and multi-chance service rule ($m = 2$).

In this paper we investigate the bifurcation of the input buffer and two possible contention/arbitration rules in the bifurcated (or multiple) input-queued ATM switch. Followed is an analysis for the throughput of a bifurcated input-queued ATM switch employing the restricted rule, as a practical solution for the bifurcated input-queued switch, through the generalization of the analysis by Karol *et al* [1]. The analysis result is compared with the simulation result over different switch sizes. Also, the analysis is extended, through simple modifications, to get the throughput bound for the bifurcated input-queued switch employing the free rule.

2. Bifurcated input-queued switches

As a heuristics of improving the limited throughput of the input-queued non-blocking packet switch with a single FIFO, *input expansion* or *input smoothing* has been studied for about a decade. These approaches provide much enhanced throughput bound by expanding input

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[†]The authors are with the Communication Network Laboratory, Department of Information and Communications, Kwang-Ju Institute of Science and Technology (KJIST), 1, Oryong-dong, Puk-gu, KWANGJU, 500-712, S.Korea. Web URL: http://charly.kjist.ac.kr/~hykim/

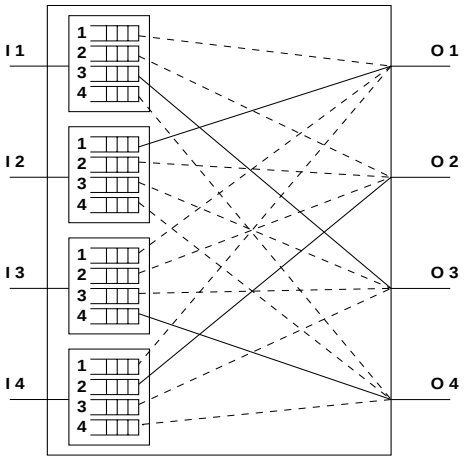

Fig. 2 A 4×4 bifurcated input-queued switch with restricted contention and single-chance service rule ($m = 4$).

ports or both input and output ports. However, they require the switch fabric expansion to exchange multiple cells in parallel.

Recently, the bifurcation approaches in input queueing are paid much attention due to the practical potential both in the switching performance and in hardware. The bifurcated (or multiple) input-queued packet switch is an idea of dividing each input buffer into m ($1 \leqq m \leqq N$) parallel buffer blocks logically or physically, so as to let each input port have more opportunities to switch a cell or cells. (The number of bifurcated buffers in an input port m is also called the bifurcation parameter.) Even though this approach requires multiple memory blocks in each input port, it can be resolved through the logical division of a buffer or the use of a common memory as discussed later.

Before we proceed to discuss the possible types of the bifurcation approach and their operation in the input-queued ATM switch, we define an *arbitration round* as an arbitration for an output port. Then, there are N arbitration rounds in a time slot for an $N \times N$ switch.[††] In the bifurcated input-queued ATM switch, all the bifurcated buffers are assumed to be able to attend the arbitration rounds for all output ports, since they are not distinguishable one another. As the result, an input port can switch up to m cells in a time slot, one from each of m bifurcated buffers, provided that the multi-cell transmission is allowed.

With the bifurcation approach, we can envision two contention and arbitration methods. First, if an input port is allowed to switch and transfer maximum m cells in a time slot, one from each bifurcated buffer, we call this kind of contention and arbitration rule *free contention* and *multi-chance service rule*, respectively. That is, a bifurcated buffer having a HOL cell continues to attend arbitration rounds until the HOL cell is selected in the same time slot. The throughput analysis for this kind of switch is found in [5] and [7] based on the analysis by Karol *et al* [1] and by Hui *et al* [2], respectively. On the other hand, if an input port is permitted to switch and transfer only one cell from one of its m bifurcated buffers, this kind of contention and arbitration rule are referred to as *restricted contention* and *single-chance service* rule, respectively. In the latter case the number of buffers within an input port is preferred to be equal to the switch size. That is, $m = N$. The number m, however, might be less than N as in [7] but this implies the renouncing of arbitration chances. The throughput bound for the case of $m = N$ will be analyzed in the following section.

In such a fashion of increasing the opportunity of serving a cell or cells in a time slot, or alleviating the probability of the HOL blocking by equipping multiple parallel FIFOs for each input port, the bifurcation approach can enhance the throughput of the ordinary input-queued switch with a single FIFO. However, this approach using multiple FIFOs is likely to have few chance of being embodied practically, viz., little practical potential, because the unscheduled nature of the arriving traffic might require much buffer space in proportion to the bifurcation parameter m. In the case of $m = N$, it requires N times buffer space per input port as much as the ordinary input-queued switch.

An easy solution for getting around the problem of the inefficiency in memory usage is to use a common buffer shared by multiple address buffers. That is, logical bifurcated FIFOs are deployed instead of physically discriminated FIFOs. In this case, the address buffer, corresponding to the bifurcated buffer itself, is still FIFO memory but requires far less memory space since it just stores couples of bytes of address information of the common memory. As the first practical perspective, we consider the free contention and multi-chance service rule in the switch equipped with a single common buffer shared by multiple address buffers in an input port. In this case, the efficiency of entire memory usage could be improved by statistical sharing of the common buffer. Challenges encountered with this approach are: (i) the internal speedup occurred in common memory access time when an input port is selected multiple times for different outputs in a time slot, and (ii) the inefficiency in the address buffer utilization when a bursty traffic destining for an specified output port arrives at input ports.

Considering the restricted contention and single-chance service rule in the switch equipped with a common buffer shared by multiple FIFO address buffers in an input port, we can find that the internal speedup is not required from the fact that an input port is restricted to send only one cell in a time slot. An exemplification of this kind of switch is found in the Random Access Input-Buffered (RAIB) switch which we pro-

[††]In some papers such as [6] and [7], an arbitration round is defined as the arbitrations for all N output ports.

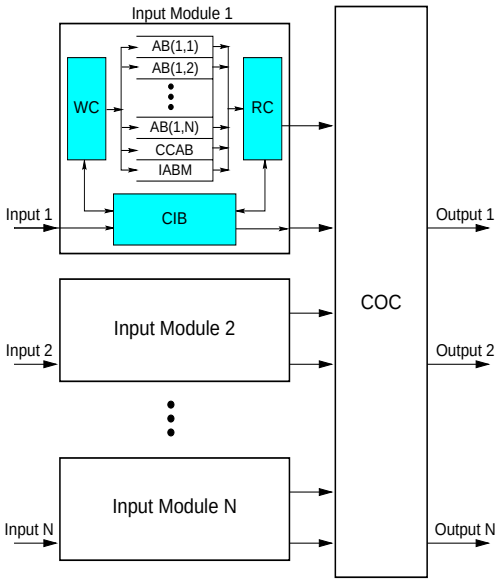

Fig. 3 An example of the bifurcated input-queued packet switch with restricted contention: Random access input-buffered (RAIB) switch in [8] and [9].

posed in [8] and [9], and the switch architecture is shown in Figure 3. In the switch architecture, the arbitration logic in the COC (common output controller) governs the arbitrations between N FIFO address buffers, so that one cell from each of the input modules is sent to its destining output through the switching fabric.

In the forthcoming section we derive the throughput bound for the bifurcated input-queued switch with the restricted contention rule when $m = N$ through the generalization of the analysis by Karol *et al* [1]. The throughput bound for the bifurcated input-queued switch with the free contention rule is also derived by simple modifications of the result obtained for the restricted contention rule.

3. Throughput analysis

We do not here retrace the analysis in [1] since the reader is assumed to be accustomed to it and the same tutorial expositions are found in the literature such as [4] and [10], etc. However, we find it expedient, for familiarity's sake, to use identical or similar notations as in those literature listed above in the following analysis for the bifurcated input-queued switch with two different contention rules.

Time is slotted and the slots carry fixed-length packets such as ATM cells. Traffic arriving at each input line is assumed to be independent, identical, and uniformly distributed over the N output ports. Assuming that there are N bifurcated buffers in an input port, traffic on each input line splits into N bifurcated buffers with the equal probability of $1/N$. In order to use the analysis in [1], each bifurcated buffer must be able to accommodate all cells for all output ports. In general, however, a bifurcated buffer stores the cells destined to the specific output ports as shown in Figures 1 and 2. Nevertheless, we can apply the analysis procedure of [1] in our analysis by the virtue of the uniformity of the arrival traffic for output ports.

Now, we model the bifurcated input-queued switch employing the restricted rule for the case of $m = N$. From the model shown in Figure 2, we can make the important observation that the $N \times N$ switch can be completely separated into N sub-switches, one sub-switch for each output. Each sub-switch is of dimension of $N \times 1$ and identical one another under the same traffic assumption as mentioned before. Therefore, the average throughput per port of the overall $N \times N$ switch is simply the throughput of any one of the $N \times 1$ sub-switches. For example, there are four 4×1 sub-switches in Figure 2. As mentioned previously, the bifurcated buffers 1 in all the four input modules serve the output port 1 exclusively and the bifurcated buffers 2 serve the output port 2 only, and so on.

The challenge in analyzing the switch employing the restricted rule is that the sub-switches interact each other in such a fashion of banning the previously selected input ports from attending arbitration rounds followed in the same time slot. It also implies that the cell selection occurs in all possible arbitration rounds with a certain probability. If the arbitration order in a time slot is assumed to be distributed uniformly, then the probability for a cell to be selected in a specific arbitration round is $1/N$ for all arbitration rounds. Therefore, the total throughput is obtained by taking expectation of the throughputs obtained in all arbitration rounds.

Using as similar notations as in [1] is most helpful for the readers to easily understand the following analysis. The definition of the notations, however, should be modified to adopt the bifurcated model for the restricted contention rule. Following the terminology in [1] as much as possible, let:

B_n^i The number of HOL cells *blocked* out of the HOL cells attending the arbitration round for output i during the nth time slot. In other words, the number of HOL cells addressed to output i, but not selected by the controller during the arbitration round for output i within the nth time slot;

A_n^i The number of cells addressed to output i which *arrive* at the head of *free* bifurcated input queues during the nth time slot. A bifurcated input queue is *free* during the nth time slot, if and only if the HOL cell of it was transmitted during the $(n-1)$st time slot;

F_n^i The number of HOL cells *freed* out of the HOL cells attending the arbitration round for output i during

the nth time slot. In other words, the number of cells transmitted to output i through the switching during the nth time slot.

The dynamics of the virtual queue of all blocked HOL cells addressed to the tagged output port i at the beginning of the time slot can be written as

$$B_n^i = max(B_{n-1}^i + A_n^i - 1,\ 0)$$

and the expected blocked cells in this *M/D/1* queue, when we consider a properly large value of N, is readily found to be

$$E[B] = \frac{\rho^2}{2(1-\rho)} \tag{1}$$

since the steady-state number of cells addressed to output i that move to the head of input queues each time slot, namely A^i, becomes Poisson with rate ρ as $N \to \infty$ [11]. Further, for a specified output port the total number of HOL cells blocked by the arbitration and by the restricted contention rule, plus the number of HOL cells that were selected for transfer to the output side, must be add up to N:

$$B_{n,k}^i + (k-1) + F_{n,k}^i = N \tag{2}$$

where k $(1 \leqq k \leqq N)$ implies the order of arbitration in a time slot, or $(k-1)$ implies the number of restricted input ports in the kth arbitration round. Note again that the term $B_{n,k}^i$ is the number of HOL cells blocked by the kth arbitration for output i in a time slot. Considering the third arbitration round ($k = 3$ or $(k-1) = 2$) in a time slot, for example, the number of blocked HOL cells by the restricted rule for output i is two and the number of blocked HOL cells by the arbitration for the output should be either $N-3$ or $N-2$ since $F_{n,k}^i$ could take either 1 (when one of the cells addressed to output i is selected for transmission) or 0. The superscript of $B_{n,k}^i$ can be omitted since B_n is statistically identical for all output ports.

Taking expectations in the limit of Equation (2) as $n \to \infty$,

$$E[B_k] + (k-1) + E[F_k] = N. \tag{3}$$

Since $E[F_k]$ is clearly the throughput of the $N \times 1$ switch per output line for the kth arbitration round, i.e., the parameter ρ_k in the earlier expression for $E[B_k]$, we immediately have

$$E[B_k] = N - (k-1) - \rho_k, \tag{4}$$

or

$$\frac{\rho_k^2}{2(1-\rho_k)} = N - (k-1) - \rho_k. \tag{5}$$

The maximum throughput ρ_k is thus found, for the kth arbitration round, to be

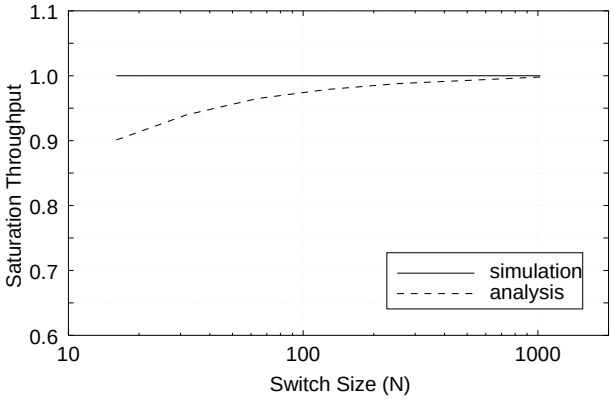

Fig. 4 Maximum attainable throughput for the bifurcated input-queued switch with the restricted contention rule (i.e., $m = N$). (by computer simulation for 10^8 time slots)

$$\rho_k = N - (k-1) + 1 - \sqrt{(N-(k-1))^2 + 1} \tag{6}$$

for $k = 1, 2, 3, \cdots, N$. Thus, the average throughput per port merely becomes

$$T = \frac{1}{N}\sum_{k=1}^{N} \rho_k \tag{7}$$

since the arbitration order is assumed to be uniformly distributed for all output ports.

In the above analysis, the closed formula (7) yields very high throughput per port ($T \approx 1.0$) for large switch size (N) as shown in Figure 4. For example, $T = 0.975$ for $N = 100$, which is a sizeable enhancement of throughput. In practice, however, the throughput obtained by the computer simulation is very close to 1.0 irrespective of the switch size N. It is noteworthy that the difference between the curves for the smaller switch size in Figure 4 is caused by the fact that the modeling of the cell arrival (A^i) as a Poisson process is not valid when the switch size is small. Hence, the analysis based on the improper cell arrival modeling is not valid for the small N. However, the cell arrival follows a Poisson process for the larger switch size, so that the difference in the throughput becomes negligibly small.

Here, let us consider the bifurcated switch employing the free rule. With the free rule, the term $(k-1)$ should be removed since there are no discriminations between arbitration rounds. So does the subscript k representing the order of arbitration round. Thus, B_n in Equation (2) should be changed into the sum of the blocked HOL cells for all output ports. So does F_n. Then, Equation (2) becomes

$$\sum_{i=1}^{N} B_n^i + \sum_{i=1}^{N} F_n^i = N \tag{8}$$

Similar operations as shown in Equation (3) through Equation (7) results straightforwardly in

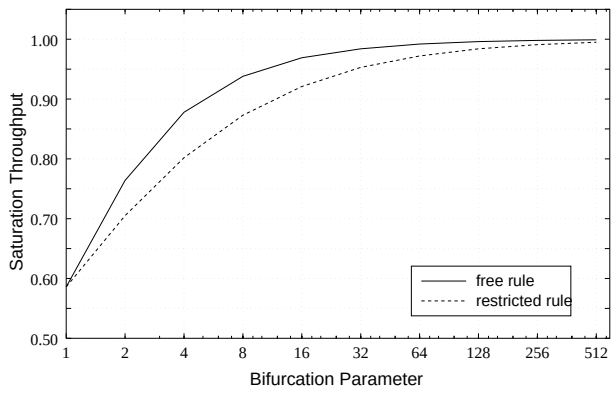

Fig. 5 Maximum attainable throughput for the bifurcated input-queued switch.

$$T = N + 1 - \sqrt{N^2 + 1} \tag{9}$$

where still $m = N$. Even though Equation (9) is obtained for the special case of $m = N$, we can think of m ranging from 1 to N for the switch with the free rule. Therefore, we can change N into m and get:

$$T = m + 1 - \sqrt{m^2 + 1} \qquad \text{for } 1 \leqq m \leqq N \tag{10}$$

which, in turn, corresponds to the throughput of the bifurcated input-queued switch employing the free rule as the function of m as in [5] and [7]. In this case, the throughput also comes to 1.0 as $m \to \infty$ when N is infinite, which is slightly higher than that of the restricted contention case since we withdraw the restriction for the pre-selected input port in the bifurcated switch with restricted contention. Figure 5 compares the saturation throughputs for both rules in terms of the bifurcation parameter m when the switch size is assumed to be infinite. As shown in the figure, the throughput bound for the free rule is slightly higher than that for the restricted rule. Setting $m = 1$ (no bifurcation) in Equation (10), in particular, we can get the well-known result that the throughput of the ordinary input-queued packet switch with a single FIFO becomes $2 - \sqrt{2}$.

4. Conclusions

In this paper, we have proposed and discussed the bifurcated (or multiple) input-queued ATM switch which equips m FIFOs in each input port. Also, we have come up with two contention/arbitration rules for the bifurcated switch. They are the free and restricted contention rules. With the free contention rule, an input port can serve up to m cells in a time slot, one from each of m bifurcated buffers. However, it results in the internal speedup in the interfaces between input modules and the switch fabric and/or in memory access when a common memory is divided logically and used as multiple buffers. With the restricted contention rule, on the other hand, an input port can serve only one cell in a time slot so that the internal speedup does not matter any further. For both rules, we analyzed the saturation throughput. At first, the saturation throughput for the bifurcated switch with the restricted rule was obtained when $m = N$. The saturation throughput for the switch with the free rule is obtained through the withdrawal of the restriction in the number of cells serviced from an input port and the generalization in the range of m. In both case, the throughput approaches to 1.0 as the switch size becomes infinite. As shown in Figure 5 the restricted rule provides slightly lower throughput bound than its counterpart. But, the bifurcated input-queued switch employing the restricted rule is considered to be more appropriate for the high-speed ATM switch, since it does not require any internal speedup or switch fabric expansion.

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